Amendments to the Claims

Please amend Claims 1, 18, and 24 through 26 such that the pending claims will read as follows:

Claim 1 (Currently Amended): A method for modeling a circuit having one or more latches comprising:

providing a timing tool that models a circuit design having latches, wherein the timing tool models each latch of the circuit design as being non-transparent;

receiving a circuit design in the timing tool, the circuit design having a plurality of latches; and

allowing a selected subset of one or more latches of the circuit design to exhibit latch transparency while the selected subset is still being modeled as non-transparent by the timing tool during modeling of ~~the~~ a timing behavior of the circuit design with the timing tool.

Claim 2 (Original): The method of claim 1 wherein receiving the circuit design having a plurality of latches comprises receiving a list of components and connections to the components included in an integrated circuit (IC).

Claims 3-17 (Canceled).

Claim 18 (Currently Amended): A computer program product for modeling a circuit having one or more latches comprising:

a medium readable by a computer, the computer readable medium having computer program code adapted to:

model a circuit design having latches, wherein each latch of the circuit design is modeled as being non-transparent;

receive a circuit design having a plurality of latches; and

allow a selected subset of one or more latches of the circuit design to exhibit latch transparency while the selected subset is still being modeled as non-transparent during modeling of a timing behavior of the circuit design.

Claim 19 (Canceled).

Claim 20 (Previously Presented): The computer program product of claim 18 wherein the computer program code adapted to receive a circuit design having a plurality of latches includes computer program code adapted to receive a list of components and connections to the components included in an integrated circuit (IC).

Claim 21 (Previously Presented): The computer program product of claim 18 wherein the computer program code adapted to allow a selected subset of one or more latches of the circuit design to exhibit latch transparency includes computer program code adapted to alter an input signal to the selected subset of one or more latches.

Claim 22 (Previously Presented): The computer program product of claim 21 wherein the computer program code adapted to alter an input signal includes computer program code adapted to prevent the input signal from reaching the selected subset of one or more latches at a time that the input signal would have otherwise reached the selected subset of one or more latches.

Claim 23 (Previously Presented): The computer program product of claim 21 wherein the input signal includes a launch clock signal.

Claim 24 (Currently Amended): A method for modeling a circuit having one or more latches comprising:

providing a timing ~~verification~~ tool adapted to model circuit designs, wherein the timing ~~verification~~ tool models latches in the circuit designs as non-transparent;

receiving a circuit design in the timing ~~verification~~ tool, the circuit design having a plurality of latches;

selecting a subset of the plurality of latches of the circuit design; and

altering a signal input to the subset of latches so that the subset of latches exhibit latch transparency during modeling of ~~the~~ a timing behavior of the circuit design even though the timing ~~verification~~ tool continues to model the subset
of latches as non-transparent.

Claim 25 (Currently Amended): The method of claim 24 wherein receiving the circuit design in the timing ~~verification~~ tool includes receiving a list of components and connections to the components included in an integrated circuit (IC).

Claim 26 (Currently Amended): The method of claim 24 wherein altering a signal input to the subset of latches includes altering an input signal to a clock input of the selected subset of one or more latches.

Claim 27 (Previously Presented): The method of claim 26 wherein altering an input signal includes preventing the input

signal from reaching the selected subset of latches at a time that the input signal would have otherwise reached the selected subset of latches.

Claim 28 (Previously Presented): The method of claim 27 wherein the input signal includes a launch clock signal.

Claim 29 (Previously Presented): The method of claim 1 wherein allowing a selected subset of one or more latches of the circuit design to exhibit latch transparency includes altering an input signal to the selected subset of one or more latches.

Claim 30 (Previously Presented): The method of claim 29 wherein altering an input signal to the selected subset of one or more latches includes preventing the input signal from reaching the selected subset of one or more latches at a time that the input signal would have otherwise reached the selected subset of one or more latches.

Claim 31 (Previously Presented): The method of claim 30 wherein the input signal includes a launch clock signal.